CONTROLLING DATA FLOW BETWEEN PROCESSOR SYSTEMS

Abstract of the Disclosure

Direct memory access data transfers may be initiated between buffers on one processor system to corresponding buffers in another processor system. The buffers in each system may be provided as a linked list such that transfers successively occur between the buffers. Each buffer may include a descriptor that indicates whether or not the buffer is full or empty. As a result, the buffer may be accessed by controllers in either processor system.